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Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is shown in Fig. 7.3. (a) Word number 723 in the memory shown in Fig. 7.3 contains the binary equivalent of 3455. Q. 1.1: List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digits. Q. 7.24: Repeat Problem 7.23, using a PAL. PAL programming table for BCD-to-Excess-3 converter. Q. 6.30: Show that a Johnson counter with n flip-flops produces a sequence of 2^n states. List the 10 Digital Design: Q. 1.10: Convert the following binary numbers to hexadecimal and to decimal: (a), (b) PLA Design problem #1 in easy way Programmable Logic Array PLA. Q. 7.8: (a) How many $32K \times 8$ RAM chips are needed to provide a memory capacity of 256Kbytes? (b) How

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Q. 7.20: Tabulate the truth table for an 8×4 ROM that implements the Boolean functions $A(x,y,z) =$

Q. 7.1: The memory units that follow are specified by the number of words times the number of bits

EEE344 Digital System Design Lab 6 Sequential Circuits (Counters and Memory Modules) Digital Logic Design (Rec. 12) Synchronous Circuits

Digital Logic - Sep - 4Q. 1.2: What is the exact number of bytes in a system that contains (a) 32K bytes, (b) 64M bytes(c)

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Q. 7.19: Tabulate the PLA programming table for the four Boolean functions listed below. Q. 2.21: Convert each of the following to the other canonical form: (a) $F(x,y,z) = g(1,3,5)$ (b) .. Q. 3.12: Simplify the following Boolean functions to product-of-sums form: (a) $F(w,x,y,z) = \text{sum}(0,1,2,$ Digital Design: Q. 1.6: The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. Q. 3.28: Derive the circuits for a three-bit parity generator and four-bit parity checker using an

Q. 5.2: Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter

Q. 5.4: A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when

Q. 4.8: Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to BCD

Q. 6.25: It is necessary to generate six repeated timing signals T0 through T5 similar to the ones

Q. 1.20: Convert decimal +49 and +29 to binary, using the signed 2's complement representation and e

Q. 7.25: The following is a truth table of a three input, four output combinational circuit

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Library of Congress Cataloging-in-Publication Data Mano, M. Morris, 1927 – Digital design : with an introduction to the verilog hdl / M. Morris Mano, Michael D. Ciletti.—5th ed.

~~Digital Design—National Institute of Technology, Srinagar~~

M. Morris Mano is an Emeritus Professor of Computer Engineering at the California State University, Los Angeles. His notable works include the Mano Machine, i.e. a theoretical computer that contains a central processing unit, random access memory, and an input-output bus. M. Morris Mano has authored numerous books in the area of digital circuits that are known for teaching the basic concepts ...

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